**Cell Description:**

This is a standard NOR cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Behavioral Verilog:**

The behavioral Verilog for the NOR is independent of its drive strength. Replace the N in the module name with the respective drive strength (i.e. 1, 2).

//Verilog HDL for "Lib6710\_06", "NOR2X2" "behavioral"

module NOR2X2 ( Y, A, B );

input A;

output Y;

input B;

nor \_i0(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| NOR2X1 | 27.0 | 7.2 |
| NOR2X1 | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
|  |  |  |

**Logic Symbol:**

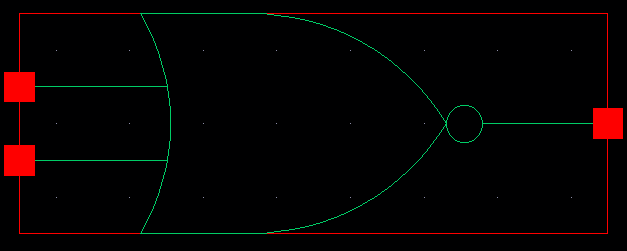
****

Figure 1: Symbol View for the NOR cell.

**CMOS Schematic:**

The following figures display the CMOS schematics for the NOR cells.

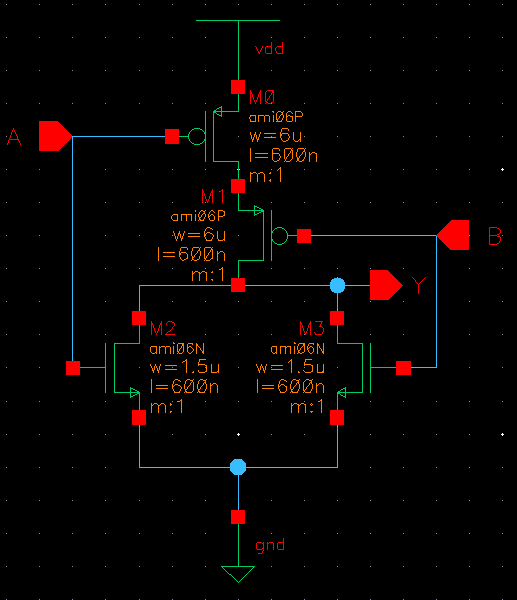


Figure 2: CMOS Schematic for the NOR2X1 cell.

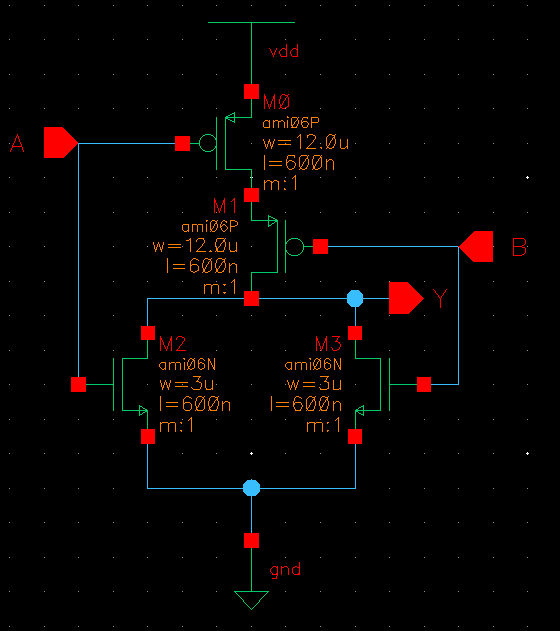


Figure 3: CMOS Schematic for the NOR2X2 cell.

**CMOS Layout:**

The following figures display the CMOS layouts for the NOR cells.

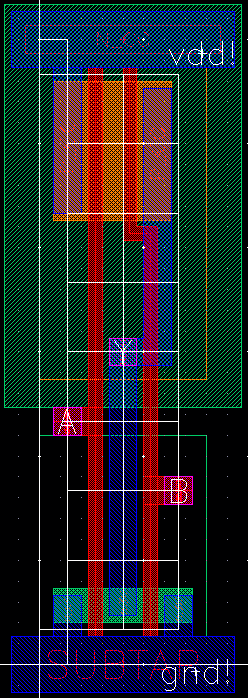
****

Figure 4: CMOS layout for the NOR2X1 cell.

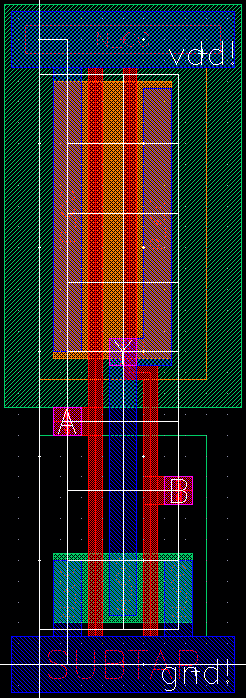
****

Figure 5: CMOS layout for the NOR2X2 cell.